PILLAR STRUCTURES

FIELD OF THE INVENTION

The present invention relates generally to fabrication of semiconductor chip interconnection, and more specifically to bump fabrication.

BACKGROUND OF THE INVENTION

In a growing market demand to improve existing semiconductor device performance on power devices, that is devices that consume a lot of energy such as amplifiers.

Current round or round-like (such as hexagonal or octagonal) solder bump interconnects have become a bottleneck to improve electrical performance to address current flow to the chip level and heat dissipation capability down to the PCB. For example, the "Advanced Connections," Spring 2002, Advanced Interconnect Technologies, issue describes, inter alia, a pillar bumping interconnect technology that uses perimeter or array flip-chip pads to connect an integrated circuit (IC) to a copper lead frame.

U.S. Patent No. 6,550,666 B2 to Chew et al. discloses a method for forming a flip chip on leadframe semiconductor package.

U.S. Patent No. 5,448,114 to Kondoh et al. discloses a semiconductor flip chip packaging having a perimeter wall.

U.S. Patent No. 6,297,551 B1 discloses integrated circuit packages with improved EMI characteristics.

U.S. Patent No. 4,430,690 to Chance et al. discloses a low inductance capacitor with metal impregnation and solder bar contact.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a improved bump design.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a die comprises a substrate and one or more pillar structures formed over the substrate in a pattern. The invention also includes the formation of a die by providing a substrate and forming one or more pillar structures over the substrate in a pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 7 schematically illustrate a preferred embodiment of the method of forming the pillar structures of the present invention.

Fig. 8 is a top down schematic view of a die on a wafer having the pillar structures of the present invention.

Figs. 9A and 9B are respective portions of Fig. 8 in dashed circles "9A" and "9B."

Figs. 10A to 10I are top down schematic views of additional dies with varying pillar structures/bumps designs/shapes.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Initial Structure

As shown in Fig. 1, structure 10 includes at least one embedded metal structure 12 and an overlying dielectric layer 14.

Structure 10 is preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

Embedded metal structure 12 may be electrically connected to one or more semiconductor devices formed within structure 10 and is preferably comprised of aluminum (Al), copper (Cu) or gold (Au) and is more preferably aluminum (Al) as will be used for illustrative purposes hereafter.

Overlying dielectric layer 14 is preferably comprised of nitride, silicon nitride (Si_3N_4), silicon oxide (SiO_2) or polyimide and is more preferably silicon nitride as will be used for illustrative purposes hereafter.

The structure of Fig. 1 may be cleaned as necessary.

Formation of Metal Layer 15 – Fig. 2

As shown in Fig. 2, a metal layer 15 is formed over the SiN layer 14. Metal layer 15 is preferably formed by sputtering.

Metal layer 15 is formed/spread over the whole of the wafer surface. Metal layer 15 preferably comprises a lower metal layer 16 and an upper metal layer 18. Lower metal layer 16 may be a metal barrier layer and is preferably titanium (Ti) or TiW and is more preferably Ti. Upper metal layer 18 is preferably copper (Cu).

Formation of Masking Layer 20 – Fig. 3

As shown in Fig. 3, a masking layer 20 is formed over metal layer 15.

Masking layer 20 is preferably comprised of photoresist.

Patterning of Photoresist Layer 20 – Fig. 4

As shown in Fig. 4, photoresist layer 20 is then patterned to form patterned photoresist layer 20′ having an opening 22 exposing a portion 24 of Cu layer 18. Opening 22 is formed in the shape selected to become the shape of the pillar structure 34. For example, as shown in the Figs., opening 22 is rectangular but may also be round, ring-shaped, bar-shaped or spline as well as other shapes.

Plating of Metal Layer 26 Within Opening 22 – Fig. 5

As shown in Fig. 5, a pillar metal layer 26 is formed over the exposed portion 24 of Cu layer 18 within opening 22 to a thickness of preferably from about 60 to 120 μm and more preferably from about 70 to 100 μm. Pillar metal layer 26 is preferably formed by plating. Pillar metal layer 26 will be in the shape selected for the pillar structure 34, for example rectangular as specifically illustrated in the Figs. or round, ring-shaped, bar-shaped, wall-like or spline or other shapes.

Pillar metal layer 26 is lead-free and is preferably comprised of copper (Cu).

The pillar metal layer 26 may be coated with, for example, oxide or another material such as chromium, nickel, etc.

An optional layer of solder 28 is formed/plated over Cu pillar layer 26. Optional solder layer 28 may be roughly flush with the top surface of the patterned photoresist layer 20' and may be overplated to preferably up to about 5 μm. Solder layer 28 is preferably comprised of: (1) from about 60 to 70% tin and from about 30 to 40% lead (Pb) for eutectic; (2) about 63% tin and 37% lead (Pb) for eutectic; (3) from about 99 to 100% tin and Sn3.5Ag for lead-free; or (4) 100% tin for lead-free and more preferably (2) about 63% tin and 37% lead (Pb) for eutectic or (4) 100% tin for lead-free.

Removal of Patterned Mask Layer 20′ – Fig. 6

As shown in Fig. 6, the remaining patterned mask/photoresist layer 20′ is removed from the structure of Fig. 5, preferably by stripping, to expose portions 30 of Cu layer 15 outboard of Cu pillar layer/solder layer 26/28.

Etching of Exposed Portions 30 of Cu Layer 15 – Fig. 7

As shown in Fig. 7, the exposed portions 30 of Cu layer 15 outboard of Cu pillar layer/solder layer 26/28 are removed, preferably by etching, to expose portions 32 of overlying SiN layer 14 outboard of Cu pillar layer/solder layer 26/28.

Reflow of Copper Pillar Layer/Solder Layer 26/28 – Fig. 7

Also as shown in Fig. 7, the wafer is subject to reflow so that the optional solder/cap layer 28 is reflowed to form pillar structure 34 of the present invention. The copper pillar layer 26 does not melt at the reflow temperature of the solder cap 28 or lead-free solder cap 28. The cap 28 is the portion that bonds the die/CSP with the substrate/leadframe/PCB.

The total height of the pillar structure 34 after reflow is preferably from about 60 to 150 μm and more preferably about 100 μm.

Solder 28′ of pillar structure 34 provides a seal over the top of the Cu pillar layer 26 while it's sides are exposed.

It is noted that the bump can be at variable heights within the die.

The pillar structures 34 are used to connect die to die, die to leadframe and/or die to substrate.

Example Die Design 100 – Figs. 8 and 9

Fig. 8 illustrates an example die design 100 employing a design of the pillar structures 34 of the present invention surrounded by the die perimeter 102. As shown in Fig .8, the die 100 may include pillar structures/bumps 34 of varying shapes.

The die perimeter 102 may be used, and provides RF shielding, in Surface Acoustic Wave (SAW) devices, noise reduction, power current capacity, hermetic shield and may be used in RF devices, power devices and MEMs for noise isolation and current capacity.

Figs. 9A and 9B are the respective portions of Fig. 8 in dashed circles "9A" and "9B." Fig. 9A illustrates example pillar structure 34 widths, lengths and spacing for rectangular shaped pillar structures 34. As shown in Fig. 9A, the pillar structures 34 of the present invention may be roughly rectangular and have a: width 42 of preferably about 289.0 μm; respective lengths 40', 40'' of preferably about 789.0 μm or about 1289.0 μm; be spaced apart lengthwise about 500.0 μm center-to-center and be spaced apart about 211.0 μm end-to-end. As shown in Fig.

9B, pillar structures 34 may be round shaped having a diameter of about 289.0 μm and be spaced apart about 500.0 μm.

Figs. 10A to 10J illustrate dies 100' having other permissible pillar structure/bump 34 shapes and designs. For example, as shown in Fig. 10D pillar structure/bump 34 may be circular and may also be a square wall-like structure 34 as shown in the center of the die 100'.

The pillar structures of the present invention may be used in Surface Acoustic Wave (SAW) devices and power switches, for example, as well as MEMs.

Advantages of the Invention

The advantages of one or more embodiments of the present invention include:

1) the pillar structures of the present invention can conduct a higher flow of current;

2) better board level reliability performance with the use of the pillar structures of the present invention;

3) C4 (control collapse chip connect) feature of the pillar structures maintain required stand-off between the die and the package;

4) the pillar structures of the present invention provide improved heat dissipation; and

5) bigger area of metal/copper in a given pad opening provides better reliability.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.